FIG. 1

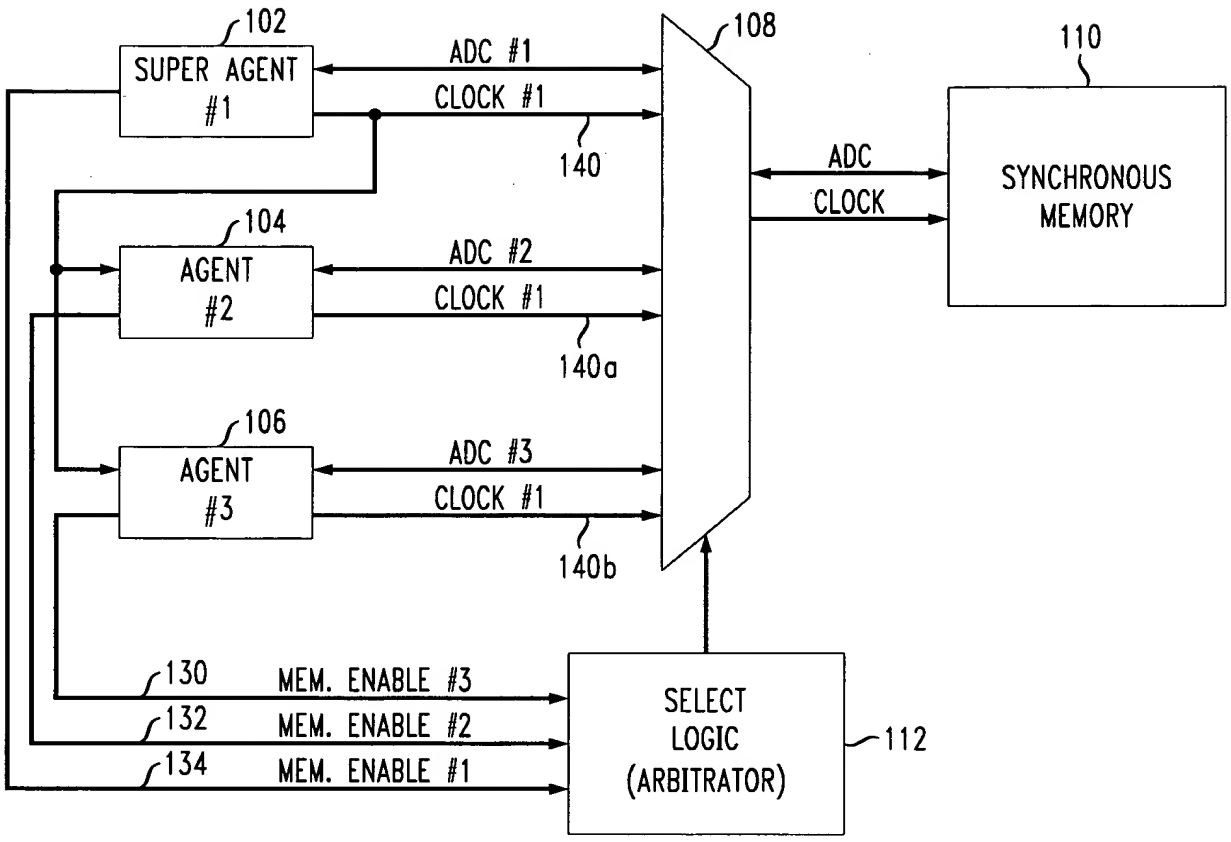
102
SUPER AGENT #1
ADC #1
CLOCK #1
140
104
AGENT #2
ADC #2
CLOCK #1
140a
106
AGENT #3
ADC #3
CLOCK #1
140b
108
110
ADC
CLOCK
SYNCHRONOUS MEMORY
130
MEM. ENABLE #3
132
MEM. ENABLE #2
134
MEM. ENABLE #1
SELECT LOGIC (ARBITRATOR)
112

FIG. 2

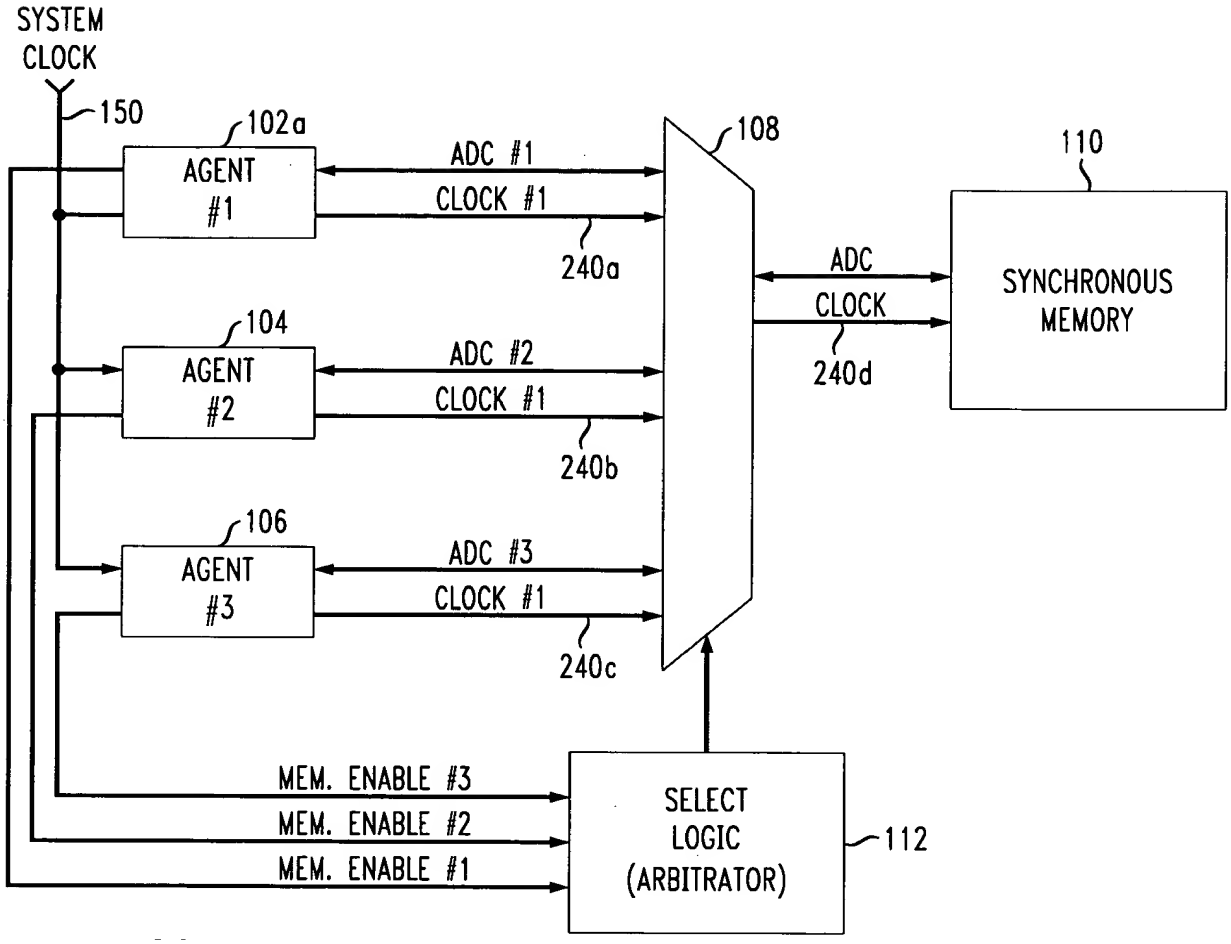
SYSTEM CLOCK
150
102a
AGENT #1
ADC #1
CLOCK #1
240a
108
110
ADC
CLOCK
240d
SYNCHRONOUS MEMORY
104
AGENT #2
ADC #2
CLOCK #1
240b
106
AGENT #3
ADC #3
CLOCK #1
240c
MEM. ENABLE #3
MEM. ENABLE #2
MEM. ENABLE #1
SELECT LOGIC (ARBITRATOR)
112

FIG. 3

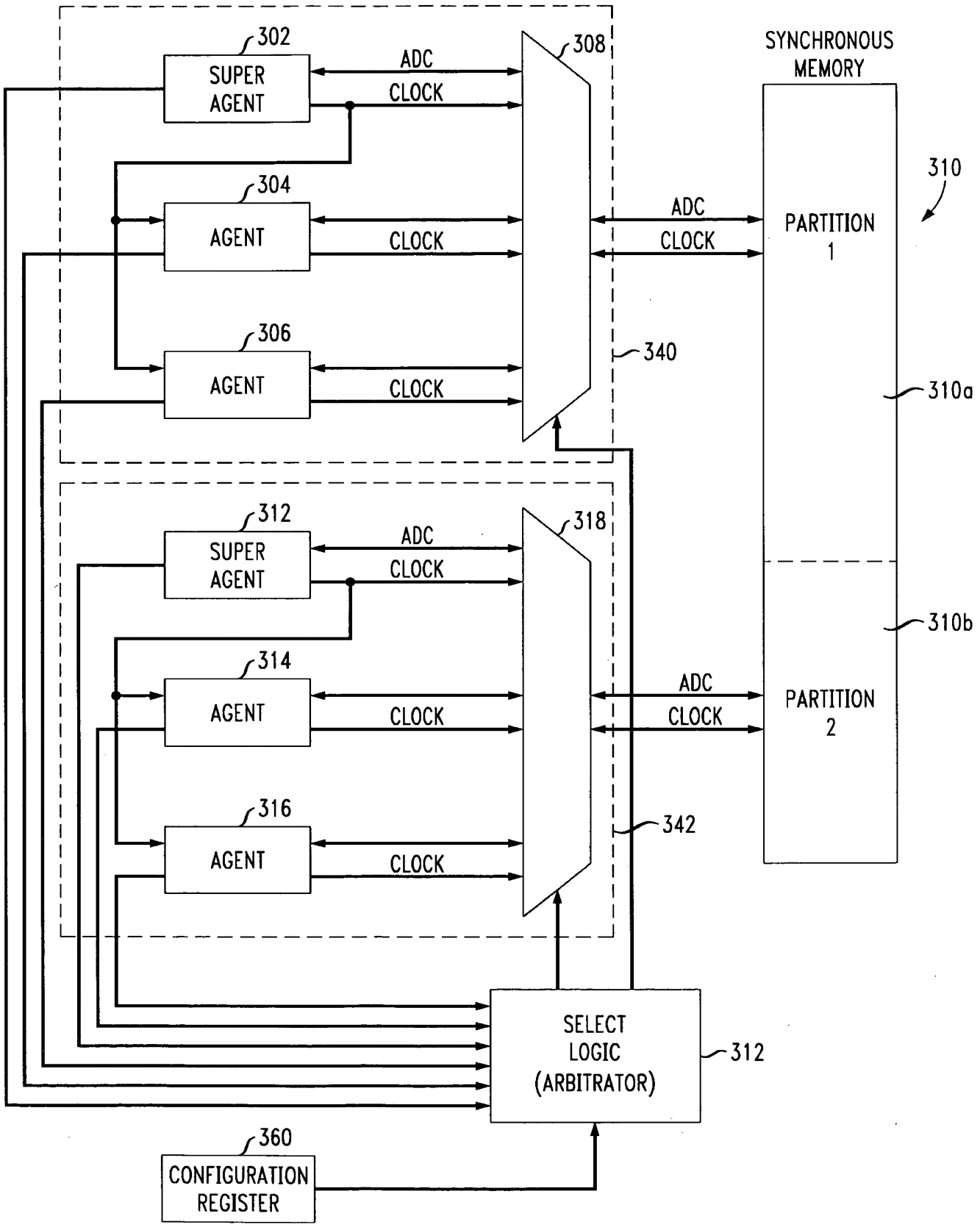
302
SUPER AGENT
ADC
CLOCK
308
SYNCHRONOUS MEMORY
310
304
AGENT
CLOCK
ADC
CLOCK
PARTITION 1
306
AGENT
CLOCK
340
310a
312
SUPER AGENT
ADC
CLOCK
318
310b
314
AGENT
CLOCK
ADC
CLOCK
PARTITION 2
316
AGENT
CLOCK
342
SELECT LOGIC (ARBITRATOR)
312
360
CONFIGURATION REGISTER

FIG. 4A

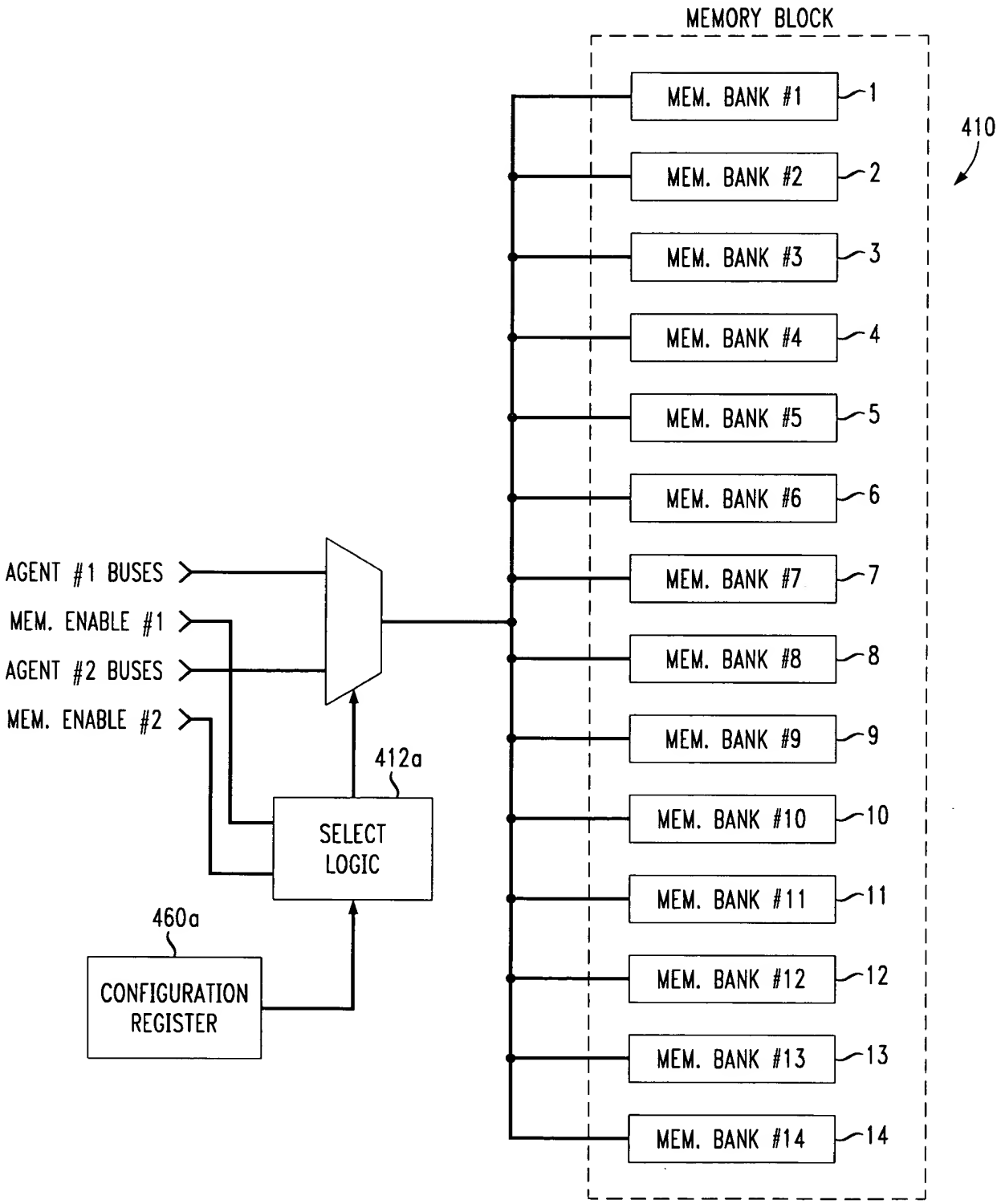
MEMORY BLOCK
410
MEM. BANK #1
1
MEM. BANK #2
2
MEM. BANK #3
3
MEM. BANK #4
4
MEM. BANK #5
5
MEM. BANK #6
6
MEM. BANK #7
7
MEM. BANK #8
8
MEM. BANK #9
9
MEM. BANK #10
10
MEM. BANK #11
11
MEM. BANK #12
12
MEM. BANK #13
13
MEM. BANK #14
14
AGENT #1 BUSES
MEM. ENABLE #1
AGENT #2 BUSES
MEM. ENABLE #2
412a
SELECT LOGIC
460a
CONFIGURATION REGISTER

FIG. 4B

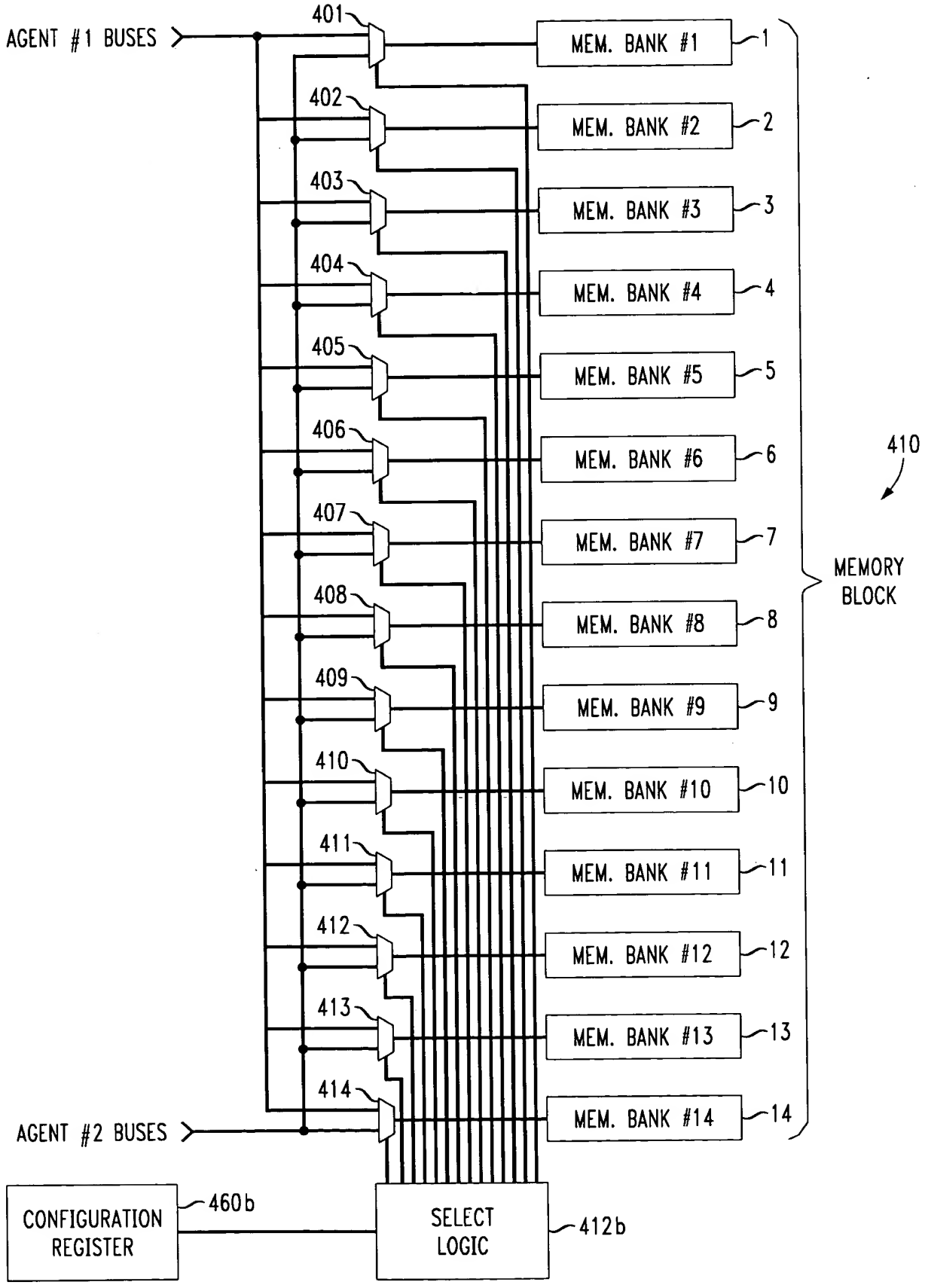
AGENT #1 BUSES
AGENT #2 BUSES
401
402
403
404
405
406
407
408
409
410
411
412
413
414
MEM. BANK #1
MEM. BANK #2
MEM. BANK #3
MEM. BANK #4
MEM. BANK #5
MEM. BANK #6
MEM. BANK #7
MEM. BANK #8
MEM. BANK #9
MEM. BANK #10
MEM. BANK #11
MEM. BANK #12
MEM. BANK #13
MEM. BANK #14
1
2
3
4
5
6
7
8
9
10
11
12
13
14
410
MEMORY BLOCK
CONFIGURATION REGISTER
460b
SELECT LOGIC
412b

FIG. 5
PRIOR ART

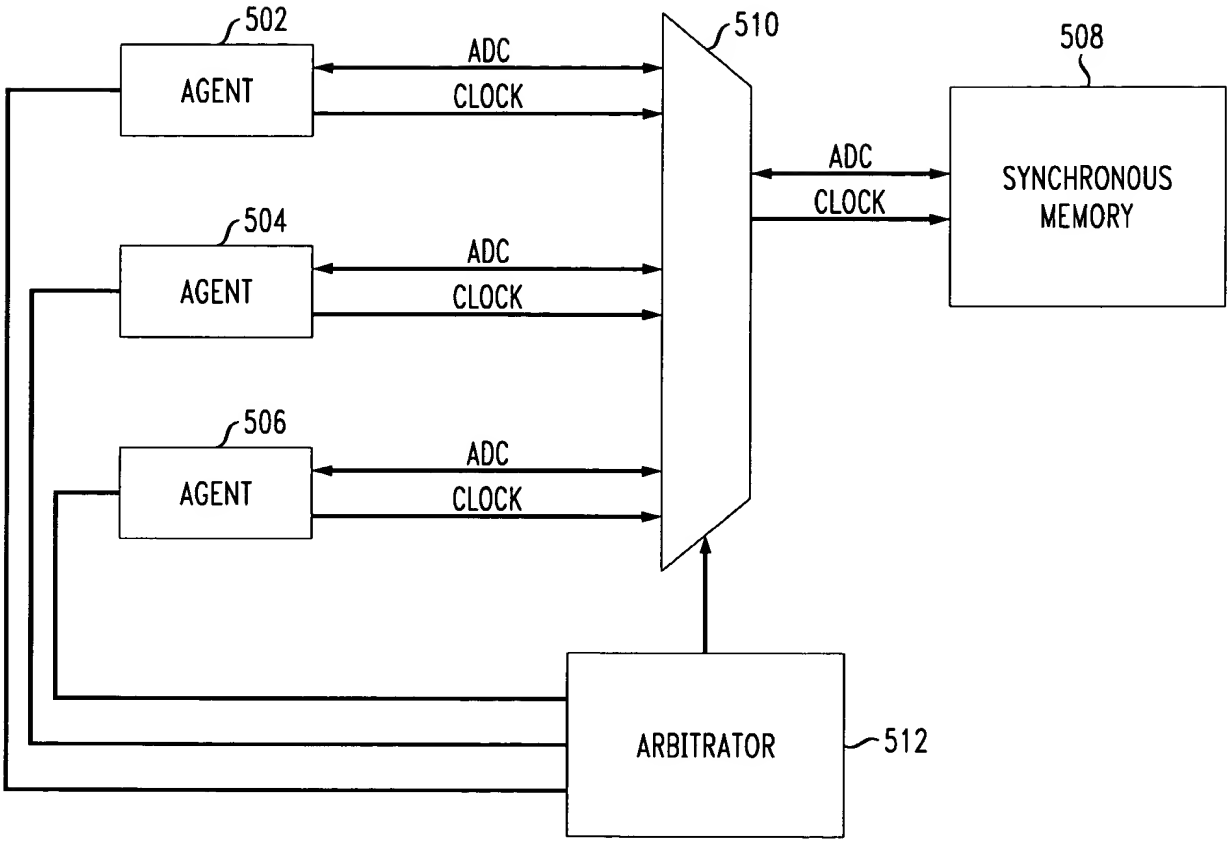

FIG. 6

PRIOR ART